

APG077N01G

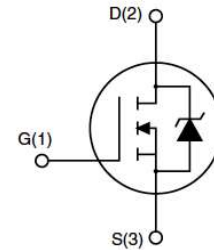
N-Channel Enhancement Mosfet

AIPOWER

DATA SHEET

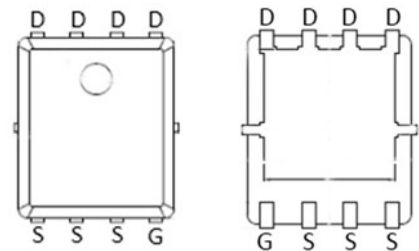
Feature

- 100V,90A
 $R_{DS(ON)} < 7.7m\Omega @ V_{GS}=10V$ (TYP:6.2m Ω)
 $R_{DS(ON)} < 10m\Omega @ V_{GS}=4.5V$ (TYP:8.0m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Application

- PWM applications
- Load Switch
- Power management



PDFN5X6-8L

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G077N01G	APG077N01G	PDFN5*6-8L	-	-	5000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ($T_a=25^\circ\text{C}$)	I_D	90	A
Continuous Drain Current ($T_a=100^\circ\text{C}$)	I_D	60	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	360	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	225	mJ
Power Dissipation	P_D	105	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.2	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~ +150	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^\circ\text{C}$ unless otherwise noted)

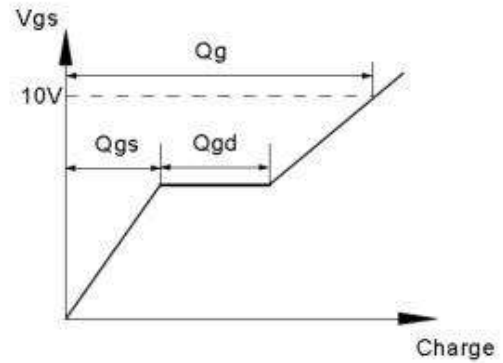
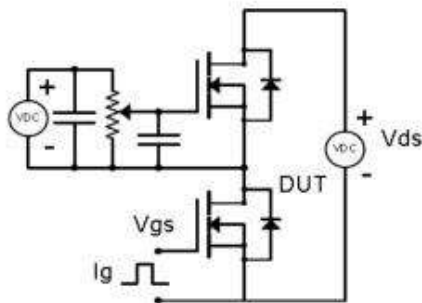
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 25V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	2.0	3.0	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 40A$	-	6.2	7.7	m Ω
		$V_{GS} = 4.5V, I_D = 40A$	-	8.0	10	m Ω
Forward Threshold Voltage	g_{fs}	$V_{DS} = 10V, I_D = 40A$	-	65	-	S
Gate Resistance	R_g	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	1.3	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	3000	-	pF
Output Capacitance	C_{oss}		-	362	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 40A,$ $V_{GS} = 10V, R_G = 3\Omega$	-	13	-	ns
Turn-on rise time	t_r		-	35	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Turn-off fall time	t_f		-	15	-	
Total Gate Charge	Q_g	$V_{DS} = 50V, I_D = 40A,$ $V_{GS} = 10V$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	10	-	
Gate-Drain Charge	Q_{gd}		-	8	-	
Reverse Recovery Charge	Q_{rr}	$I_F = 40A, di/dt = 100A/\mu s$	-	90	-	nC
Reverse Recovery Time	T_{rr}	$I_F = 40A, di/dt = 100A/\mu s$	-	60	-	ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{GS} = 0V, I_S = 20A$	-	-	1.3	V
Diode Forward current ⁽⁴⁾	I_S		-	-	60	A

Notes:

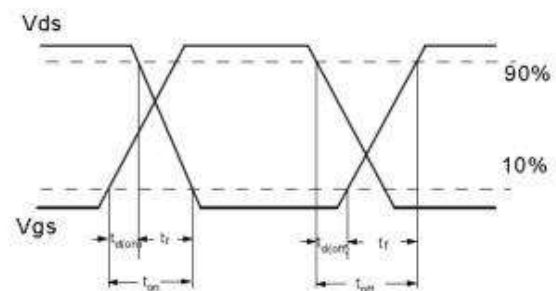
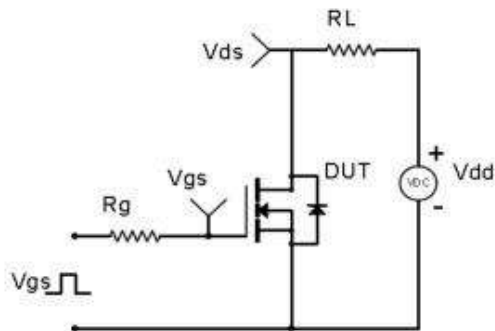
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^\circ\text{C}, V_{DD} = 50V, R_G = 25\Omega, L = 0.5mH, I_{AS} = 30A$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

Test Circuit & Waveform

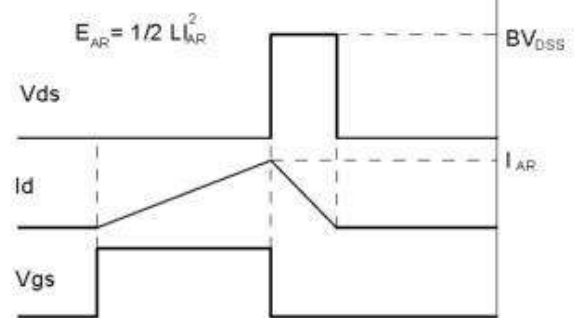
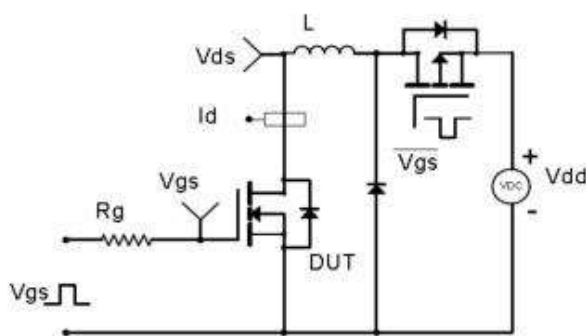
Gate Charge Test Circuit & Waveform



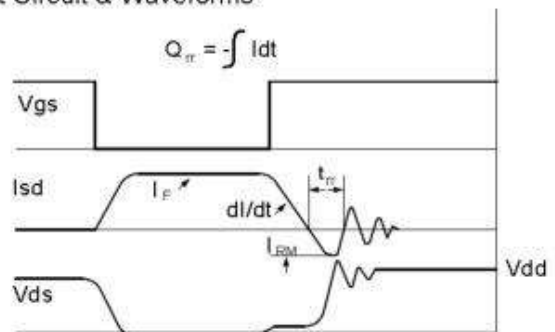
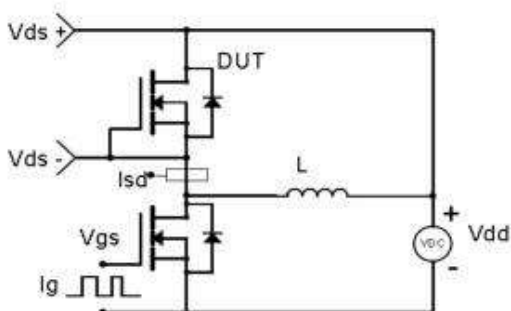
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Performance Characteristics

Fig.1 Power Dissipation Derating Curve

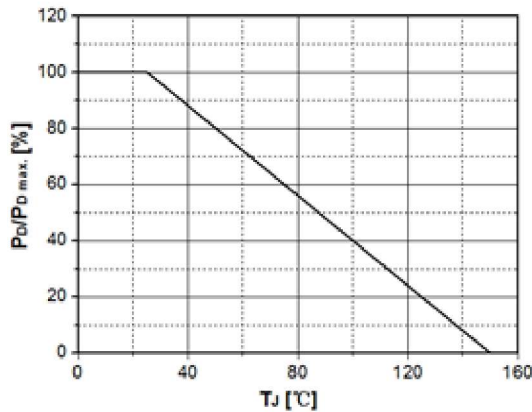


Fig.2 Avalanche Energy Derating Curve vs. Junction Temperature

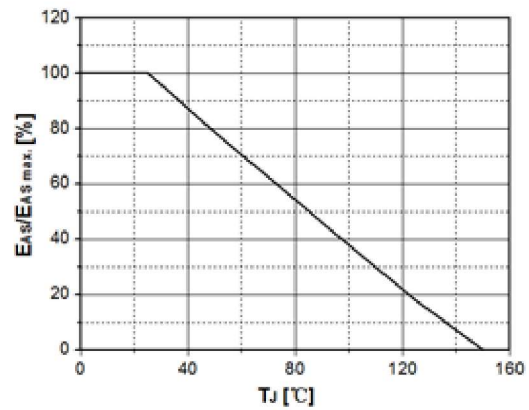


Fig.3 Typical Output Characteristics

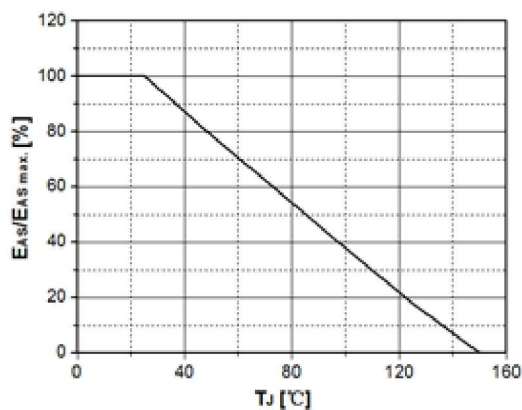


Fig. 4 Transconductance vs. Drain Current

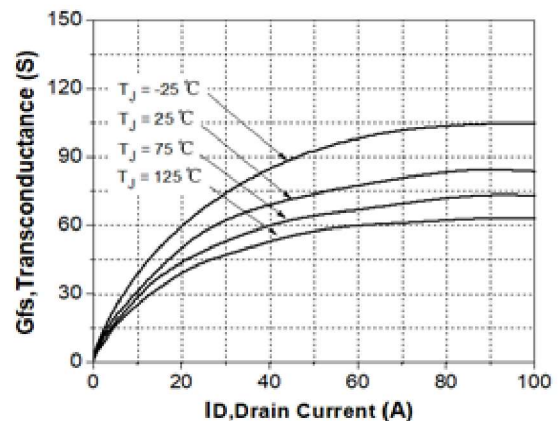


Fig.5 Typical Transfer Characteristics

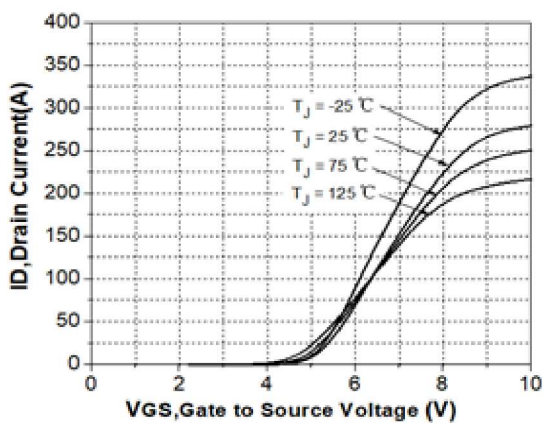


Fig. 6 State Resistance vs. Drain Current @-25°C

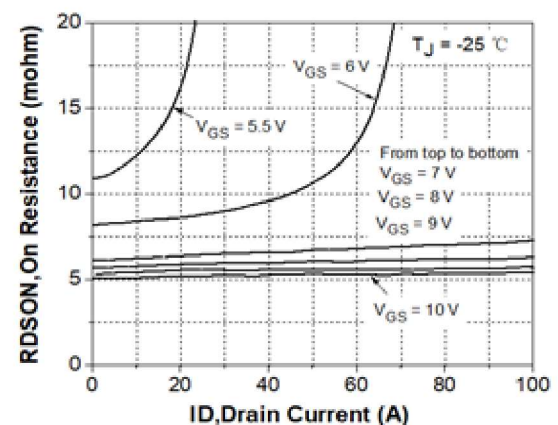


Fig.7 State Resistance vs. Drain Current @25°C

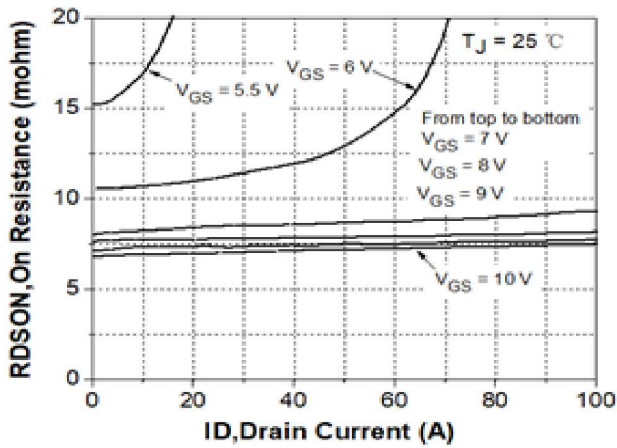


Fig. 8 State Resistance vs. Drain Current @125°C

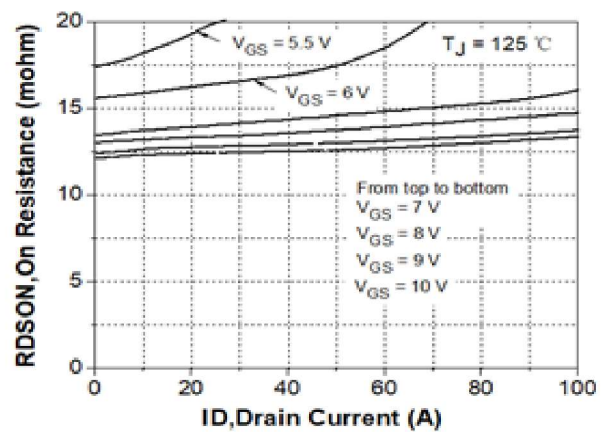


Fig.9 Typical Capacitance vs. Drain Source Voltage

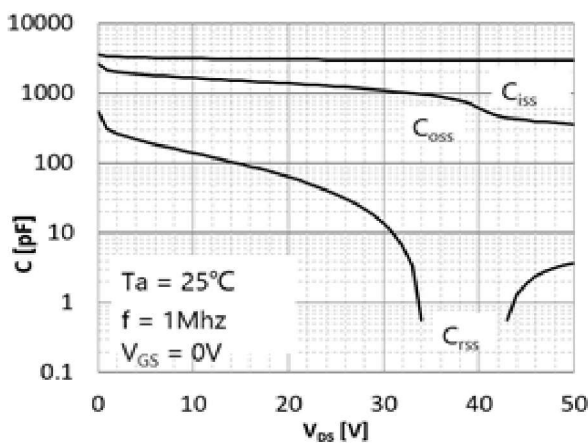


Fig.10 Dynamic Input Characteristics

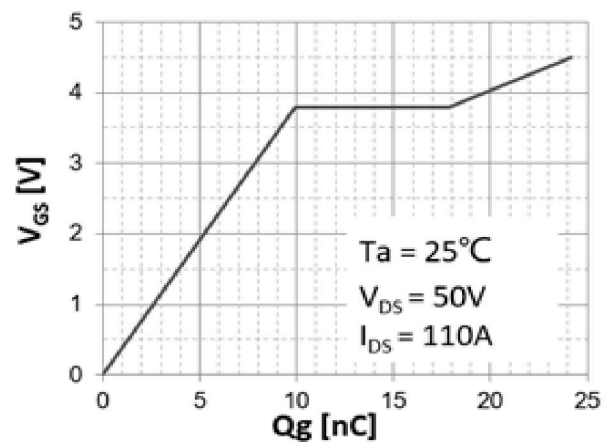


Fig.11 Breakdown Voltage vs. Junction Temperature

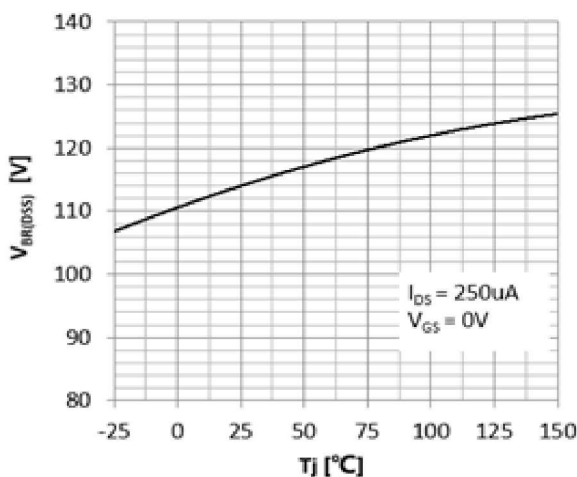


Fig. 12 Gate Threshold Voltage vs. Junction Temperature

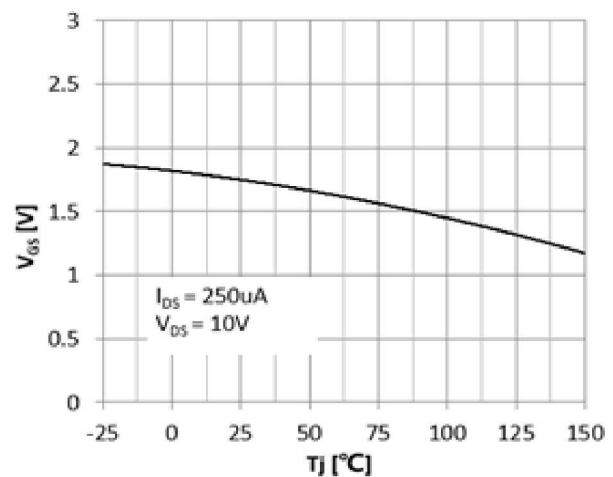


Fig.13 Safe Operating Area

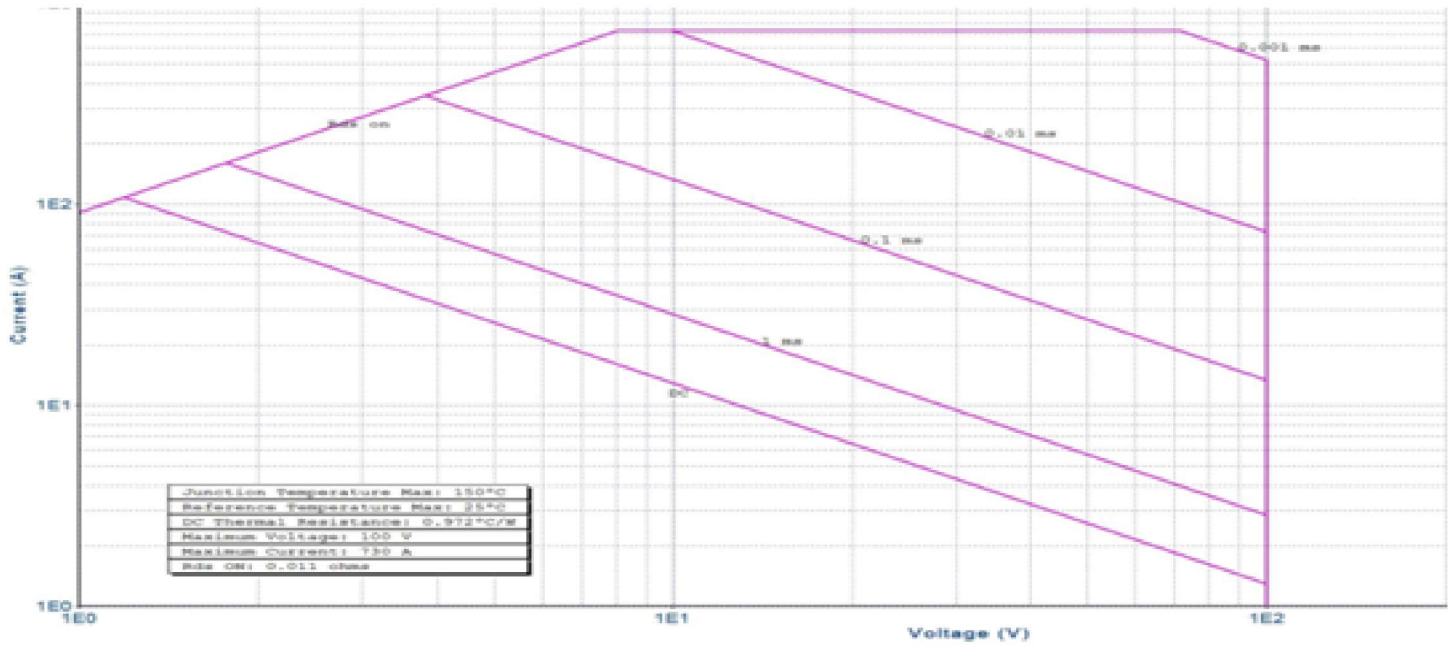
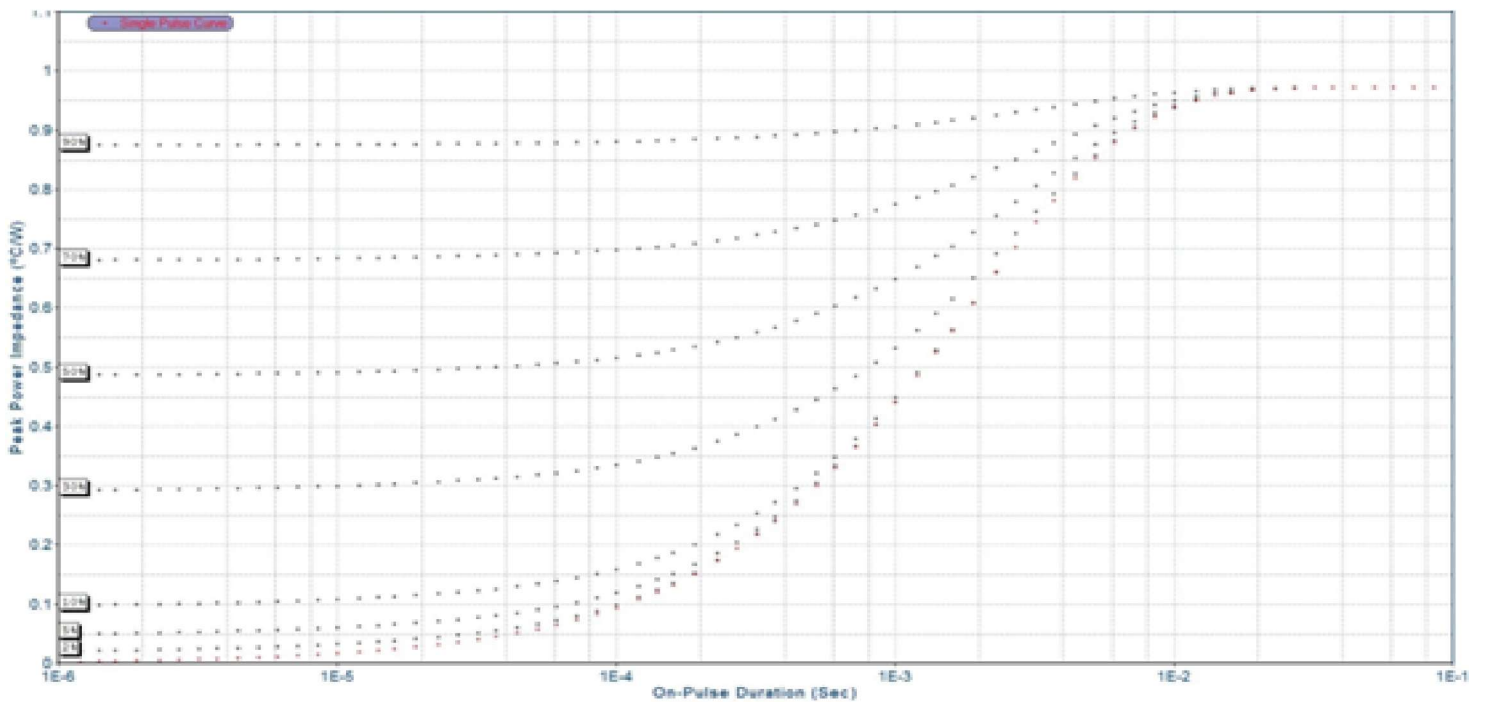
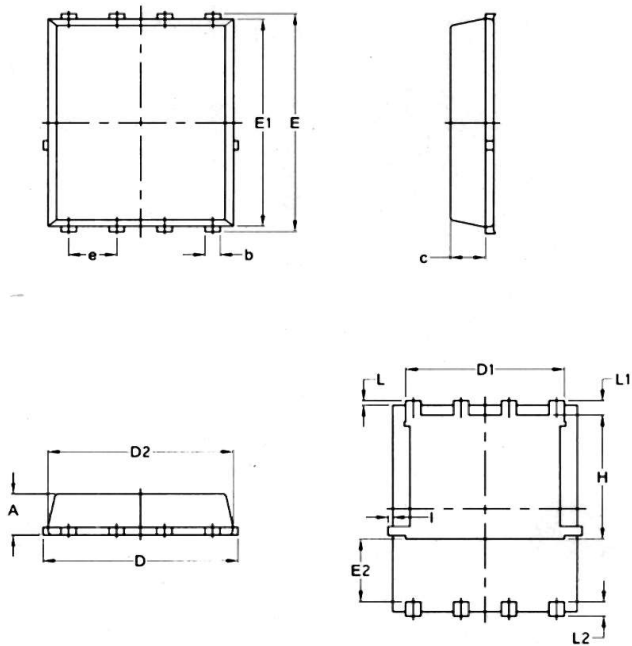


Fig. 14 Transient Thermal Response Curve



PDFN5*6-8L Package Information



PDFN5X6-8L

SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070