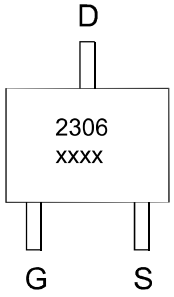
GENERAL DESCRIPTION

The AP2306E is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

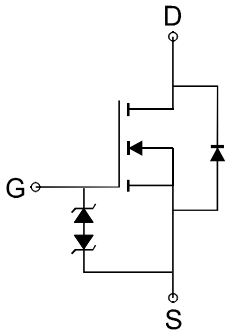
(SOT-23)

Top View



FEATURES

- $R_{DS(ON)} \leqq 31m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 52m\Omega @ V_{GS}=4.5V$
- ESD Protected
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability



APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Load Switch
- Halogen-free
- Marking:2306

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain*	T_A=25℃	I_D	5.3	A
	T_A=70℃		4.2	
Pulsed Drain Current		I_{DM}	21.2	A
Maximum Power Dissipation*	T_A=25℃	P_D	1.39	W
	T_A=70℃		0.89	
Operating Junction Temperature		T_J	-55 to 150	℃
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	1.5	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 6.7A		26	31	mΩ
		V_{GS}=4.5V, I_D= 5.0A		40	52	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHZ		370		pF
Coss	Output Capacitance			68		
Crss	Reverse Transfer Capacitance			21		
Rg	Gate Resistance	f=1MHz		1.9		Ω
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=6.7A		12		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=6.7A		5.7		
Qgs	Gate-Source Charge			3.0		
Qgd	Gate-Drain Charge			2.1		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1.0A, V_{GEN}=10V R_G=6Ω		9.2		ns
tr	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			33		
t_f	Turn-Off Fall Time			3.7		

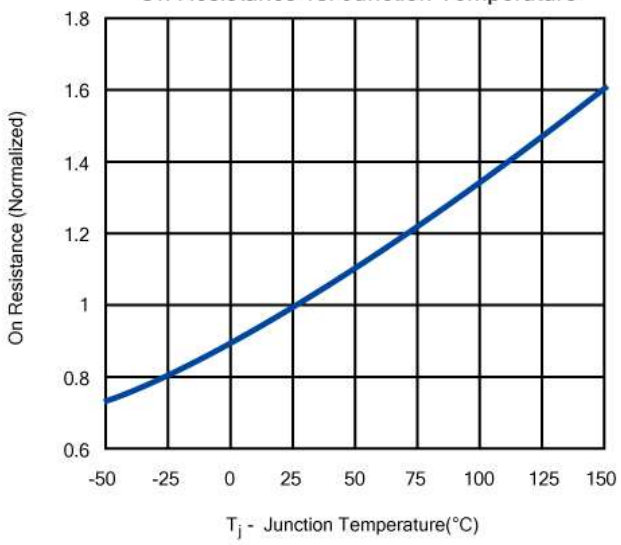
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

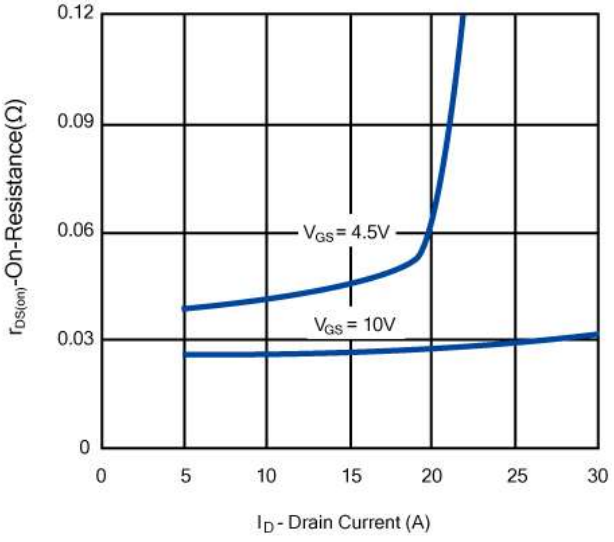
N-Channel Power MOSFET

RATING AND CHARACTERISTICS CURVES

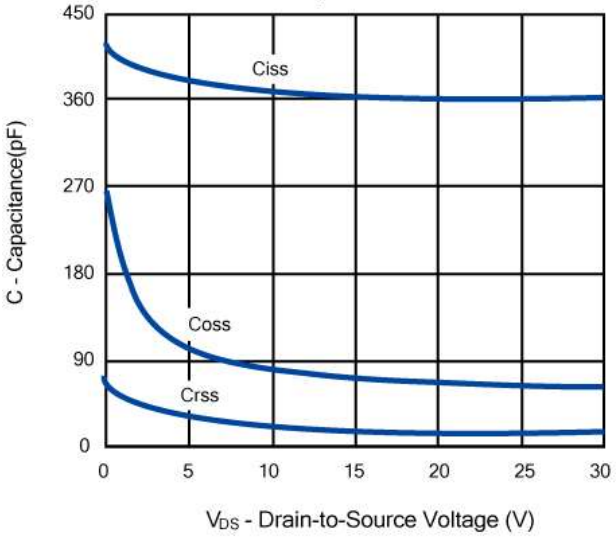
On Resistance vs. Junction Temperature



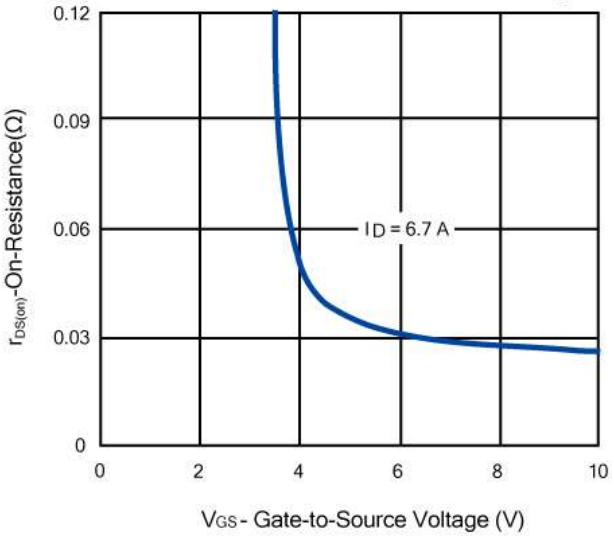
On-Resistance vs. Drain Current



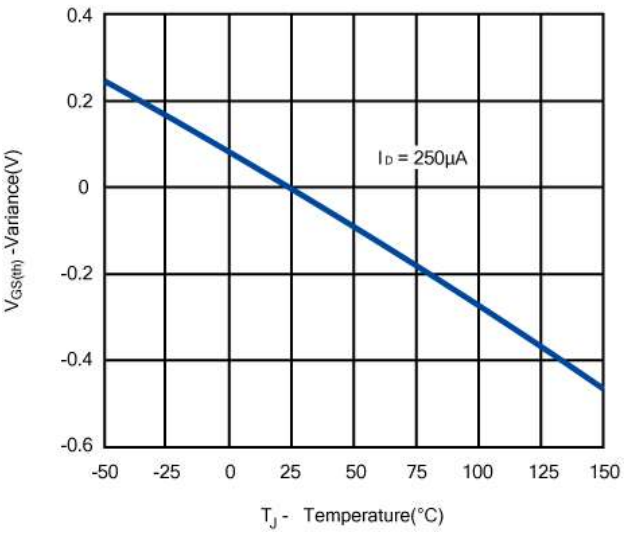
Capacitance



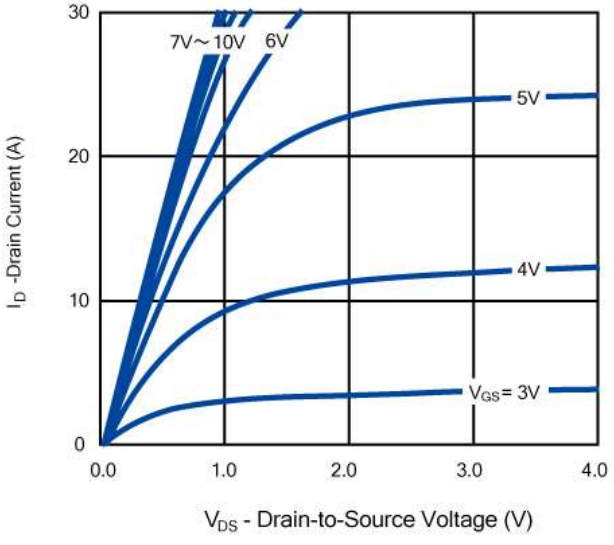
On-Resistance vs. Gate-to-Source Voltage



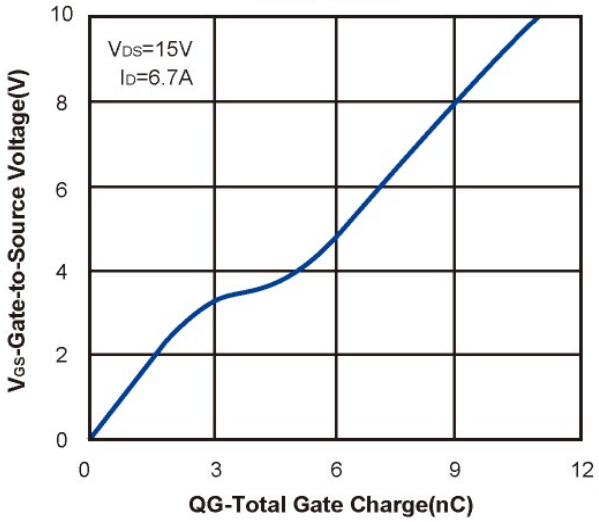
Threshold Voltage



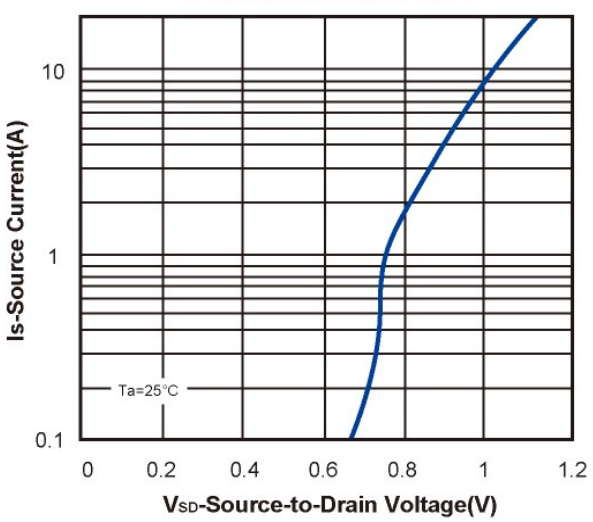
On-Region Characteristics



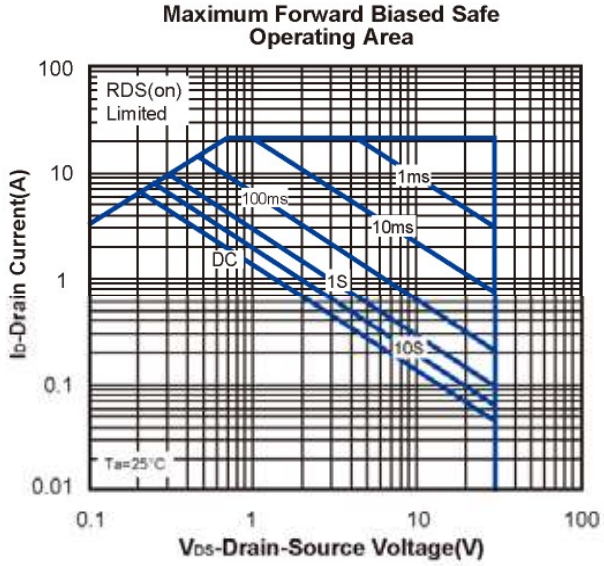
Gate Charge



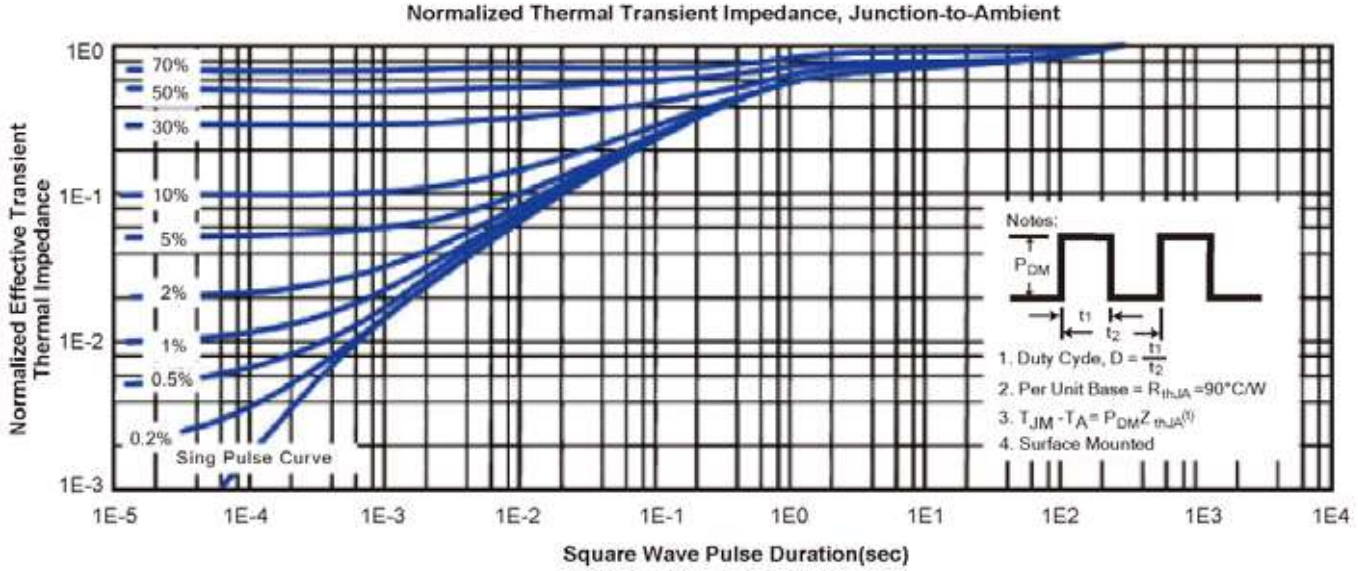
Body-diode characteristics



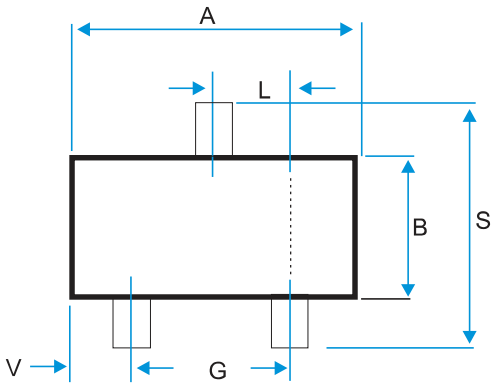
Maximum Forward Biased Safe Operating Area

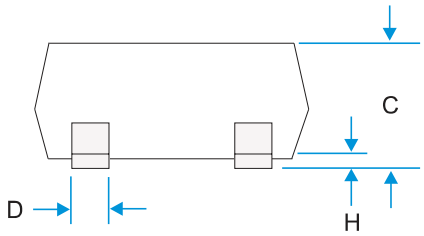


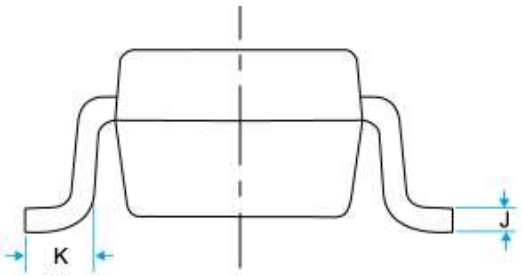
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60